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Question Paper Code : 51224

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2013.

Sixth Semester

Electronics and Communication Engineering

EC 1354 – VLSI DESIGN

(Common to Electrical and Electronics Engineering)

(Regulation 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define threshold voltage of MOS transistor.

2. Draw small signal model for an MOS transistor.

3. Give the expression for inductance of a conductor on a chip.

4. Define delay time.

5. What do you mean by super buffer?

6. What is stick diagram?

7. Develop block diagram of 4:1 MUX using instanced 2:1 MUX.

8. Write verilog behavioural description of a positive edge triggered D flip flop.

9. Distinguish between behavioural modeling and data flow modeling.

10. What is test bench?

PART B — (5 × 16 = 80 marks)

11. (a) Discuss in detail about second order effects of MOS transistor. (16)

Or

(b) Explain in detail about basic CMOS technology. (16)

12. (a) (i) An inverter uses FETs with $\beta n = 2.1mA/v2$ and $\beta p = 1.8mA/v2$. The threshold voltages are given as $V_{Tn} = 0.60V$ and $V_{TP} = -0.70V$ and the power supply has a value of $V_{DD} = 5V$. The parasitic FET capacitance at the output node is estimated to be $C_{FET} = 74fF$.

(1) Find the midpoint voltage V_M.

(2) Find the values of R_n and R_p.

(3) Calculate the rise and fall times at the output when $C_L = 0$.

(4) Calculate the rise and fall times at the output when the external load of value C_L=115fF is connected to the output. (8)

(ii) Discuss in detail about DC and transient characteristics of CMOS inverter. (8)

Or

(b) (i) Sketch the VTC of a CMOS inverter and explain the different regions of operation. (8)

(ii) Explain the concept of dynamic CMOS design. (8)

13. (a) (i) Explain in detail the capacitance estimation in MOS devices. (8)

(ii) Write notes on charge sharing. (8)

Or

(b) (i) Discuss in detail about power dissipation in MOS transistor. (8)

(ii) Write detailed notes on scaling. (8)

14. (a) (i) Draw the circuits for P_i and G_i needed for a 4 bit Carry look ahead adder in each of the following CMOS technologies:

(1) Static CMOS; (2) Domino CMOS and (3) TG logic. (10)

(ii) Construct a 2 × 2 array multiplier circuit with latching inputs. Write a Verilog description for the above circuit. (6)

Or

(b) Consider the 4 — bit shift register shown in Figure.1. The data stream D consists of sequential bits d0, d1, d2, and d3. The timing is set such that the first bit d0 enters stage 0 on the first clock edge. On the next rising edge, d1 enters stage 0, while d_0 moves to stage 1, and so on.

(i) Write a Verilog description of the shift register using DFF modules as primitives.

(ii) Select a CMOS design techniques for the DFFs and use it to construct the circuit.

(iii) Now write a verilog description of the shift registers using nMOS and pMOS primitives.

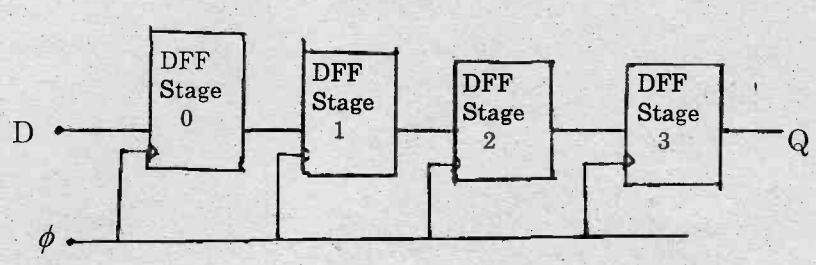

fig. 1

15. (a) Explain in detail about hierarchical modeling concepts with suitable examples in VHDL. (16)

Or

(b) (i) Explain the Task and functions in VHDL with an examples. (8)

(ii) Briefly explain dataflow and behavioural level modeling in VHDL. (8)